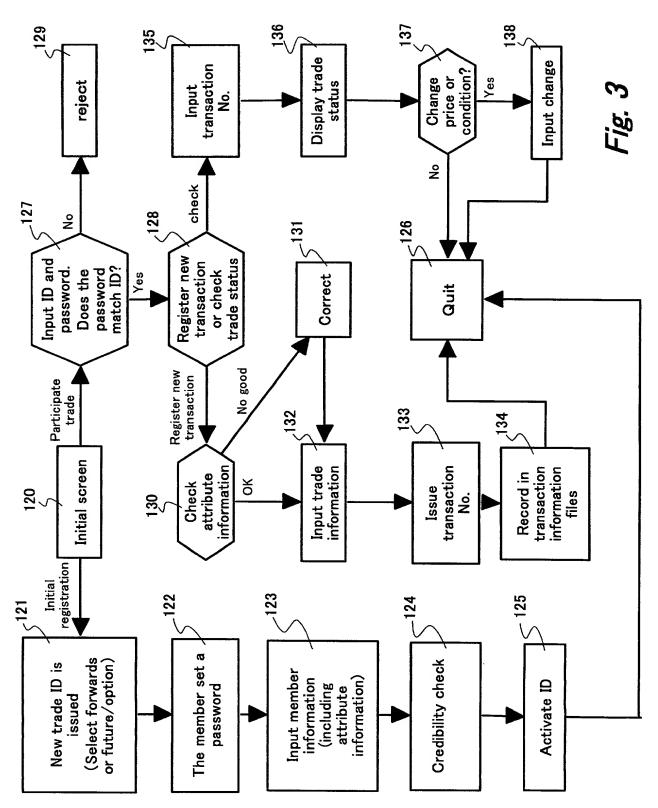


Fig. 2



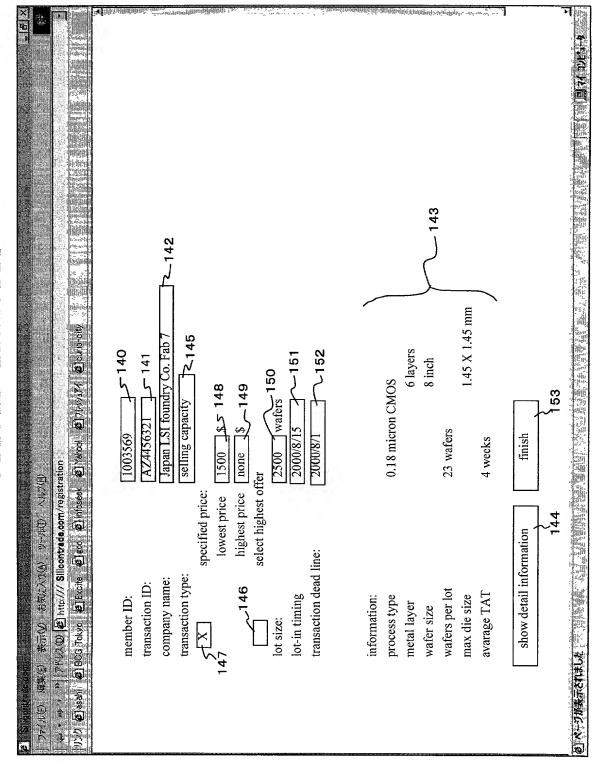


Fig. 4

member ID: 1003569

company name: Japan LSI foundry Co. Fab 7

manufacturing line information:

wafer size8 inchwafers per lot23 wafersmax die size1.45 X 1.45 mmaverage yield for TEG87.6%avarage TAT4 weeksmax capacity10000 wafers/month

process parameters:

process type
gate length
gate type
metal pitch
metal layer
metal layer
min. pad pitch
30 micron
30 micron

transistor threshold(P) 0.14 V
transistor threshold(N) 0.16 V
switching delay 400 p sec
max. clock rate 800MHz

suply voltage 1.25V max gate size 5 million

Fig. 5

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ルヴェスルブ(出) e.com/registration/process type 色 Intoseek を引がnoc をPDががが、をJuniocity を	1003569	continue to next page
2) Billiopidade com ファイルロ・編集日 表示型 お気に入り扱 ツールの ヘルグ出 シャ・き・ 2 アドレスの 個 http:///Sillicontrade.com/registration/orocess.type リング 観 sain(包号G rokyo 個 医xere 創 poc 側 misses 個 Yano) 個 P p/m	member ID: company name: Japp manufacturing line information wafer size wafers per lot max die size average yield for TEG avarage TAT max capacity process type gate length gate length gate type metal type metal type metal layer min. pad pitch transistor threshold(N) transistor threshold(N)	Continu

Fig. 6

	② ページが表示を和ました
finish	
2000	dead line
delta sigma A/D converters(30Msps) 500,000 units	number of chips
oscilator, PLL,	analog IP
1.2 million ARM7TDMI DRAM5121 1940	gate size dioital IP
1.8 V	suply voltage
800 MHz	max. clock rate
Artisan 265 pins	used library I/O signals
0.18 micron CMOS	process type
Japan Compter Systems Co.	company name:
1013644	member ID:
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Fig. 1

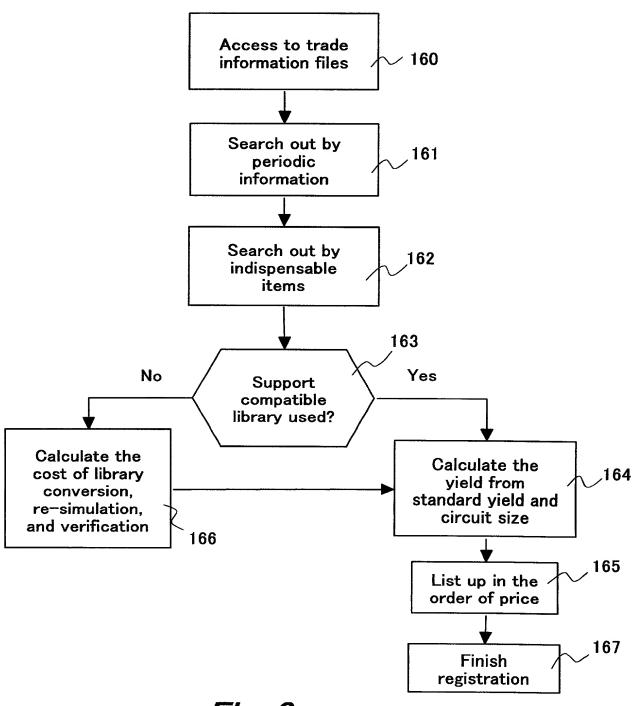


Fig. 8

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	past design Bluetooth base band AAA AAA AAA AAA
	member ID: 1020031 company name: Tokyo IP Design Co.
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	2) Silvayarda Sate

Fig. 9